

REVISION HISTORY

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| C2 | Initial Release | 11/30/2017 |
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IMPEDANCE CONTROLLED SIGNALS

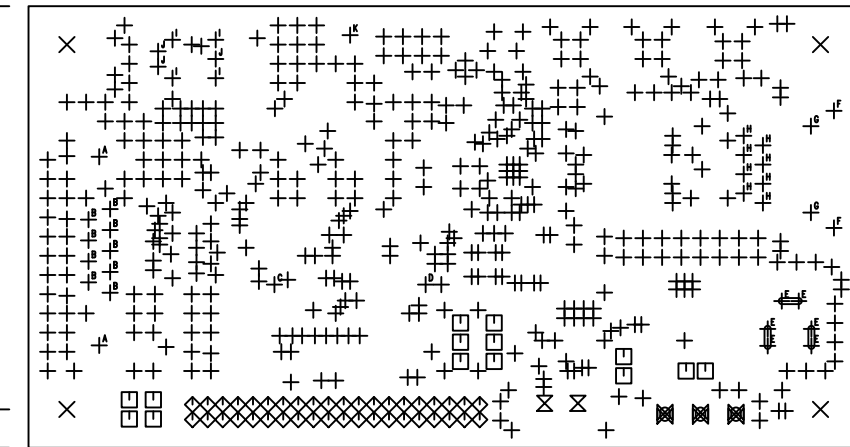
| Signal & Pairs | Trace Width | Impedance Requirement | Signal Layers | Reference Layer |
|--|--|-----------------------------|------------------------|--|
| ERX+/- ETX+/- IEXRX+/- IEOTX+/- ERXP/M ETXP/M | 8.5 MIL TRACE ~16 MIL GAP 10.1 MIL TRACE 19.9 MIL GAP | 100 Ohm +/-10% differential | Layer 1 Layer 2 | Layer 2; no ref where void Layer 3; no ref where void |
| USB+/- EXTUSB+/- | 8.5 MIL TRACE ~8.1 MIL GAP | 90 Ohm +/-10% differential | Layers 1 | Layers 2 |
| All others | 8 MIL | 50 Ohm +/-10% single-ended | Layers 1&4 | Layer 2; no ref where void Layer 3; no ref where void |

| SIZE | QTY | SYM | PLATED | TOL |
|--------------|-----|----------------|--------|----------|
| 0.01 | 463 | + | YES | +/-0.003 |
| 0.175 | 4 | X | YES | +/-0.005 |
| 0.04 | 14 | □ | YES | +/-0.003 |
| 0.0315 | 40 | ◇ | YES | +/-0.003 |
| 0.03543 | 2 | ⊠ | NO | +/-0.003 |
| 0.05 x 0.07 | 3 | ⊠ ^A | YES | +/-0.003 |
| 0.125 | 2 | ⊠ ^B | YES | +/-0.005 |
| 0.047 | 9 | ⊠ ^B | YES | +/-0.003 |
| 0.06299 | 1 | ⊠ ^C | NO | +/-0.003 |
| 0.04331 | 1 | ⊠ ^D | NO | +/-0.003 |
| 0.032 x 0.12 | 3 | ⊠ ^E | YES | +/-0.003 |
| 0.062 | 2 | ⊠ ^F | YES | +/-0.003 |
| 0.128 | 2 | ⊠ ^G | NO | +/-0.003 |
| 0.035 | 8 | ⊠ ^H | YES | +/-0.003 |
| 0.0935 | 4 | ⊠ ^I | NO | +/-0.003 |
| 0.039 | 3 | ⊠ ^J | NO | +/-0.003 |
| 0.09843 | 1 | ⊠ ^K | YES | +/-0.003 |

2.300

0.200

0.000



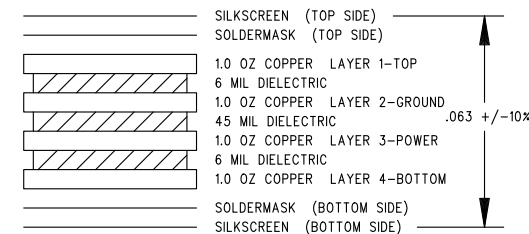
0.000

0.200

4.325

Notes: apply unless specified otherwise.

1. Material: Polyclad PCL-FR-370HR or equivalent. Overall thickness = .063" +/-10%
2. Unless otherwise specified, all hole dimensions apply after plating.
All plated through holes to have a minimum of .001" copper.
3. All holes shall be located within .003" diameter of true position. Layer to layer registration shall be within .003". All holes surrounded by land shall have a minimum annular ring of .001". All via in pads must be filled with THP-100DX1 material.
4. Apply soldermask over bare copper, color GREEN; mask shall meet IPC-SM-840 to a thickness specification of 5 um to 18 um.
5. All exposed copper shall be coated with electroless nickel/immersion gold finish. Nickel plating shall be 118-275u" thick over copper. Gold plating shall be 2-8u" thick over nickel. Boards shall pass solderability testing per J-STD-003. There shall be no evidence of exposed copper.
6. Warp or twist of board shall not exceed .010 inch per inch.
7. Silkscreen using non-conductive epoxy ink. Color: WHITE.
8. Remove all burrs and break all sharp edges.
9. Board shall meet the requirements of UL796 with a flammability rating of 94V-0.
Vendor's UL logo or designation shall be located on the solder side of board.
10. Fabricate in accordance with ANSI/IPC-A-600, class 2.
11. Dimensions and tolerances per ASME Y14.5M.
12. Fabricate using artwork 330-333-GBR Rev C2.
13. Any rework shall be to IPC-R-700C guidelines and tested per section VI. Test results shall be included with each shipment. Reworked items shall be separated from non-reworked items and the outer packaging labeled as "reworked items enclosed".
14. Tent all vias both sides.
15. All materials and processes must be RoHS compliant.

LAYUP DETAIL
4 LAYER

Lantronix

TITLE:

FABRICATION DRAWING
XPICO 240 Eval Board

| | | |
|----------|--------------------------|---------------|
| DWG A | DWG NO: 330-333-FAB-R | REV: C2 |
| SIZE | SCALE: 1 : 1 | SHEET: 1 OF 1 |